Amendments to the Specification:

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] Metallic silicides have recently become popular for use as low-resistivity trace material. Tungsten silicide ("WSi_x") has become a leading low-resistivity trace material. Various etching chemistries have been developed to pattern the WSi_x to form such conductors as the digitlines or wordlines used in memory devices (see ~~commonly~~ commonly owned U.S. Patent 5,492,597, hereby incorporated herein by reference). Other metallic silicides used in gate stacks include cobalt silicide ("$CoSi_x$"), molybdenum silicide ("$MoSi_x$"), and titanium silicide ("$TiSi_x$"). These metallic silicides have lower resistivity and are easier to fabricate than other conductors used for this purpose. However, metallic silicides are prone to oxidization. Furthermore, the metal components of the metallic silicides react chemically when they contact other elements. These properties present several problems, including degradation of the semiconductor element and peeling of the metallic silicide film. To compensate for these problems, a polysilicon layer is usually disposed between a gate dielectric layer and the metallic silicide film, and a dielectric cap layer is usually disposed above the metallic silicide film to isolate the metallic silicide.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] FIGS. 14-19 illustrate, in cross section, a conventional method of forming a gate stack having a metallic silicide film layer. FIG. 14 illustrates a gate dielectric layer 204 such as silicon dioxide (SiO_2) grown (by oxidation) or deposited (by any known industry standard technique, such chemical vapor deposition or the like) on a silicon substrate 202. A polysilicon layer 206 is formed on top of the gate dielectric layer 204, as shown in FIG. 15. The polysilicon layer 206 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 16, a metallic silicide film 208 is deposited on the polysilicon layer 206. The structure is then subjected to a heat treatment for about 30 minutes at a temperature between about ~~850°C. and 950°C.~~ 850°C and 950°C for activation of the impurities in the polysilicon layer 206 and to

anneal the metallic silicide film 208. The heat treatment temperature level is dictated by the temperature required to anneal the metallic silicide film 208. The annealing of the metallic silicide film 208 is used to reduce its resistivity.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] As shown in FIG. 17, a silicon dioxide cap 210 is then deposited on the metallic silicide film 208 at temperatures over ~~600°C.~~ 600°C by chemical vapor deposition ("CVD"), low pressure chemical vapor deposition ("LPCVD"), or the like. A resist 212 is then formed and patterned on the silicon dioxide cap 210, as illustrated in FIG. 18. The layered structure is then etched and the resist 212 is stripped to form a gate stack 214, as illustrated in FIG. 19. However, this etching results in pitting on the gate dielectric layer 204. This pitting is illustrated in FIG. 20 wherein a plurality of pits 216 is distributed on the gate dielectric layer 204 between the gate stacks 214.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] In situations where a high temperature heat cycle (cap deposition and/or annealing) is required, an ion implantation into the metallic silicide film can be performed to amorphize the metallic silicide film (i.e., disperse the silicon clusters back into the metallic silicide film) before masking and etching. The implantation ions can be silicon, tungsten, argon, or the like, or a dopant (phosphorous, arsenic, boron, and the like). The implantation can be performed before and/or after the cap deposition. The implantation energy is preferably between about 20 keV and 200 keV. The ion dose ranges from between about $1E^{13}$ and $1E^{16}$. The implantation energy and dose depend on the metallic silicide film thickness, the metallic silicide composition (i.e., ratio of silicon to metal component), the anneal heat cycle temperature, and the implantation ion used. However, it is preferred that the peak of the implantation occur at about the middle of the metallic silicide film. Furthermore, it is preferred that the dopant ion (phosphorous, arsenic, boron, and the like) amorphize the metallic silicide film. For example, for a metallic silicide film which is about ~~1800Å~~ 1800 Å thick and annealed at about ~~850°C.~~ 850°C

for about 30 minutes, a phosphorous implantation at about 75 keV and $1E^{15}$ is required to amorphize the metallic silicide.

Please replace paragraph number **[0018]** with the following rewritten paragraph:

[0018] It is, of course, understood that if a lower resistivity in the metallic silicide is required for a specific application, the gate stack can be subjected to a heat cycle after gate stack etching to anneal the metallic silicide in the gate stack. However, if the gate stack is annealed after formation, the anneal temperature must be increased by about ~~30°C. to 50°C.~~ 30°C to 50°C to achieve the same resistivity.

Please replace paragraph number **[0029]** with the following rewritten paragraph:

[0029] A cap 110, preferably including silicon nitride, is then deposited on the metallic silicide film 108, as shown in FIG. 4. The deposition of the silicon nitride layer is carried out at between about ~~400°C. and 600°C.~~ 400°C and 600°C, and preferably at about ~~500°C.~~ 500°C, by CVD (including LPCVD, APCVD, and PECVD), sputtering, spin-on techniques, or the like. In a preferred embodiment, the deposition of the silicon nitride is accomplished by plasma-enhanced chemical vapor deposition. It is, of course, understood that the cap 110 can include other dielectric material, such as silicon dioxide, as long as it deposited at temperatures below about 600°C.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] FIGS. 7-13 illustrate an alternate method, in cross section, of forming a gate stack of the present invention. The steps of the alternate method are similar to the method illustrated in FIGS. 1-6; therefore, components common to both FIGS. 1-6 and FIGS. 7-13 retain the same numeric designation. FIG. 7 illustrates a gate dielectric layer 104 grown or deposited on a silicon substrate 102. A polysilicon layer 106 is formed on top of the gate dielectric layer 104, as shown in FIG. 8. The polysilicon layer 106 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 9, a metallic silicide film 108 is deposited

on the polysilicon layer 106. A cap 110 is then deposited on the metallic silicide film 108, as shown in FIG. 10. The structure 118 (FIG. 11) is subjected to a heat cycle either to anneal the metallic silicide film 108 prior to depositing the cap 110, to form the cap 110 with a high temperature process (i.e., over ~~600° C.~~ 600°C), or both, such that silicon clusters 116 are formed in the metallic silicide film 108.